Vidya Pratishthan's Kamalnayan Bajaj Institute of Engineering and Technology, Baramati

Department of Electronics and Telecommunication Engineering

Honor Courses E&TC Engineering 2024-25

HONORS Subject of Electronics and Telecommunication Engineering
Honors in VLSI Design and Technology

2024 Pattern –S.Y. EnTC

Sem	Subject Code	Subject	Subject Credits	Teaching Scheme				Examination Scheme						Credits			Total
								Theory			Practical/ Tutorial						
				WL Type	TH	PR	TUT	Activity	ISE	ESE	TW	PR	OR	TH	PR	Tut	
III	ET24281	Advanced Digital Design	3	TP	2	2	-	10	20	50	20	20	-	2	1	-	3
IV	ET24291	ASIC Design and SoC	3	TP	2	2	-	20	20	50	20	20	-	2	1	-	3
V	ET24381	System Verilog for Design and Verification	4	TP	3	2	-	20	20	70	20	20	-	3	1	-	4
VI	ET24391	Advanced Verification Methodologies and scripting	4	TP	3	2	-	20	20	70	20	20	-	3	1	-	4
VII	ET24234	Advanced CMOS VLSI Technology	4	TP	3	2	-	20	20	70	20	20	-	3	1	-	4

SD Biradar
Autonomy Coord.

Dr. JS Rangole
HOD-E&TC

Dr. SM Bhosle
Dean Academics

Dr. SB Lande
Principal

Head
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Principal
Vidya Pratishthan's
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Vidyanagari, Baramati-413133

VPKBIET BARAMATI Affiliated to S.P.P.U. Pune Id No./PU/PN/Engg./152/2000 PUNE (MS.)

HONORS Subject of Electronics and Telecommunication Engineering
Honors in VLSI Design and Technology

2023 Pattern –T.Y. EnTC

Sem	Subject Code	Subject	Subject Credits	Teaching Scheme				Examination Scheme						Credits			Total
								Theory			Practical/ Tutorial						
				WL Type	TH	PR	TUT	Activity	ISE	ESE	TW	PR	OR	TH	PR	Tut	
III	ET23281	Advanced Digital Design	3	TP	2	2	-	10	20	50	20	20	-	2	1	-	3
IV	ET23291	ASIC Design and SoC	3	TP	2	2	-	20	20	50	20	20	-	2	1	-	3
V	ET23381	System Verilog for Design and Verification	4	TP	3	2	-	20	20	70	20	20	-	3	1	-	4
VI	ET23391	Advanced Verification Methodologies and scripting	4	TP	3	2	-	20	20	70	20	20	-	3	1	-	4
VII	ET23234	Advanced CMOS VLSI Technology	4	TP	3	2	-	20	20	70	20	20	-	3	1	-	4

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PUNE (MS.)

ET23281:- Advanced Digital Design (SEM III)

Teaching Scheme:	Credits	Examination Scheme:
Theory: 02 Hours/Week Practical: 02 Hours/Week	03	Activity:10 Marks In Sem: 20 Marks End Sem:50 Marks Practical: 20 Marks Teamwork: 20 Marks

Prior knowledge of

1. Digital Logic Design

is essential.

Course Objectives:

1. To use Verilog HDL and thus model tasks & functions at the behavioral level.
2. To Apply the state machines approach to design digital circuits.
3. To illustrate combinational circuits and sequential circuits using Verilog
4. Explain the types of programmable logic devices and building blocks of FPGA families and Implement digital circuits on FPGA

Course Outcomes:

1. Write Verilog HDL code and thus model tasks & functions at the behavioral level
2. Design the state machines using D and JK Flip Flops and model using Verilog
3. To model combinational circuits and sequential circuits using Verilog.
4. Differentiate FPGAs and Implement digital design on FPGA

Course Contents

Unit I: Verilog HDL (06 Hrs.)

Data Flow & Structural Modeling-Lexical Conventions - Ports and Modules – Operators - Gate Level Modeling - Data Flow Modeling - System Tasks & Compiler Directives - Test Bench. Behavioral level Modeling- Procedural Assignment Statements- Blocking and Non-Blocking Assignments -Tasks & Functions - Useful Modeling Techniques.

Unit II: State Machine Design (06 Hrs.)

Definition of state machines -State machine as a sequential controller- Analysis of state machines using D and JK flip-flops - Design of state machines- State table and State assignment - Transition/excitation table - excitation maps and equations - logic realization- Design examples, FSM Verilog modeling of Sequence detector - Serial adder - Vending machine. Design Guidelines for Sequential Circuits.

Unit III: Combinational Circuits and Verilog Modelling (06 Hrs.)

Adders: Ripple Carry Adder, Carry Look-Ahead Adder, Higher Bit Adders Using CLA, Carry Skip Adder, Carry Increment Adder, Carry Select Adder, Carry Save Addition, Multipliers: Sequential Multiplication, Array Multipliers, Booth's Multiplication, Multiplication Using Look-Up Table Sequential Circuits: BCD up-down counter, Synchronous and Asynchronous FIFO – Single port and Dual port ROM and RAM.

Unit IV: FPGA Architecture and Design Flow (06 Hrs.)

Types of Programmable Logic Devices: PLA, PAL, CPLD, FPGA Architecture, Programming Technologies, Chip I/O, Programmable Logic Blocks, Fabric and Architecture of FPGA. Impact of logic block functionality on FPGA performance, Model for measuring delay.

FPGA Families: Artix, Kintex, Virtex, EDA tools, Design Flow, FPGA Design Guidelines.

Text Books:

1. Samir Palnitkar, Verilog HDL, 2nd Edition, Pearson Education, 2009.

2. Advanced Digital System Design A Practical Guide to Verilog-based FPGA and ASIC Implementation.

Reference Books:

1. Data sheets of Artix-7, Kintex-7, Virtex-7.

2. Digital Logic Design Using Verilog, Coding and RTL Synthesis by Vaibhav Taraate, Second Edition Springer

3. Advanced Digital Logic Design using Verilog, State Machines & Synthesis for FPGA - Sunggu Lee, Cengage Learning, 2012.

NPTEL:

1. Digital Design with Verilog By Prof. Chandan Karfa, Prof. Aryabartta Sahu | IIT Guwahati https://onlinecourses.nptel.ac.in/noc24_cs61/preview

2. System Design Through VERILOG By Prof. Shaik Rafi Ahamed | IIT Guwahati https://onlinecourses.nptel.ac.in/noc21_ee97/preview

List of Laboratory Experiments/Assignments

1. Introduction to FPGA design flow using Verilog with a multigate IC.
2. Design and implementation of Adder and compare the performance with other adder circuits.
3. Design and implement a multiplier and compare its performance with other multiplier circuits.
4. Design and implement BCD up-down counter.

5. Design and implement FIFO.
6. Design and implement Serial adder/Sequence Detector/Vending Machine.
7. Mini Project: Design and implement Microcontroller OR Communication Protocol or any equivalent design on BASYS 3 Kit. A group of 4-5 students will design the individual project modules and integrate the complete design.

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Autonomy Coord.	HoD – E&TC	Dean Academics	Principal

VPKBIET BARAMATI PUNE (MS)

Vidya Pratishthan's Kamalnayan Bajaj Institute of Engineering and Technology, Baramati

Department of Electronics and Telecommunication Engineering

Honor Courses E&TC Engineering 2024-25

HONORS SUBJECT DETAILS

Sem	Subject Code	Subject	Subject Credits	Teaching Scheme				Examination Scheme							Workload			Total WL
								Theory			Practical/ Tutorial							
				WL Type	TH	PR	TUT	Activity	ISE	ESE	TW	PR	OR		TH	PR	Tut	
III	ET23281	Advanced Digital Design	3	TP	2	2	-	10	20	50	20	20	-		2	8	0	10
IV	**ET23291**	**ASIC Design and SoC**	**3**	**TP**	**2**	**2**	**-**	**20**	**20**	**50**	**20**	**20**	**-**		**2**	**8**	**0**	**10**
V	ET23381	VLSI Verification and Testing	4	TP	3	2	-	20	20	70	20	20	-		3	8	0	11
VI	ET23391	Scripting Languages and Verification	4	TP	3	2	-	20	20	70	20	20	-		3	8	0	11
VII	ET23481	Advanced CMOS VLSI Technology	4	TP	3	2	-	20	20	70	20	20	-		3	8	0	11
	Total:		**18**		**13**	**10**	**-**	**90**	**100**	**310**	**100**	**100**	**-**		**19**	**64**	**0**	**53**
					23			**500**			**200**				**700**			
					Internal:			**290**			**41.4**			**%**				
					External			**410**			**58.6**			**%**				

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VPKBIET BARAMATI PUNE (MS.)

ET23281:- ASIC Design and System on Chip (SEM IV)

Teaching Scheme:	Credits	Examination Scheme:
Theory: 02 Hours/Week Practical: 02 Hours/Week	03	Activity:20 Marks In Sem: 20 Marks End Sem:50 Marks Practical: 20 Marks Teamwork: 20 Marks

Prior knowledge of

1. Digital Logic Design

is essential.

Course Objectives:

CO1: Analyze the working principles and design techniques of digital CMOS circuits

CO2: Apply fabrication technology concepts, including layout design and design issues

CO3: Design and evaluate System on Chip (SoC) architectures

CO4: Explore and implement emerging trends in ASIC and SoC design,

Course Outcomes:

1. To provide a fundamental understanding of ASIC design principles and System-on-chip (SoC) architecture.
2. To familiarize students with the design flow of digital integrated circuits using CAD tools.
3. To introduce practical skills for implementing designs using Micro wind, MATLAB, and PYNQ boards.
4. To bridge the gap between theoretical knowledge and practical applications in VLSI and embedded systems.

Course Contents

Unit I: Digital CMOS Circuits (06 Hrs.)

Types of ICs: Full Custom, Semi-Custom, and Programmable Logic Devices. Types of ASICs: Standard Cell-Based, Gate Array-Based, Full Custom Design.

MOSFET parasitic, Technology scaling, Channel length modulation, Hot electron effect, Velocity saturation. CMOS Inverter, Device sizing, CMOS combinational logic design, Power dissipations, Power delay product, Body Effect, Rise and fall times, Latch-Up effect, Transmission gates.

Unit II: Fabrication Technology for ASICs (06 Hrs.)

Lambda rules, Design Rule Check, Fabrication methods of circuit elements, Layout of cell, Library cell designing for NAND & NOR, Circuit Extraction, Electrical Rule Check, Layout Vs. Schematic, Post-layout Simulation and Parasitic extraction, Design Issues like Antenna effect, Electro migration effect, Cross talk and Drain punch through, Timing analysis.

Unit III: System on Chip (SoC) Design (06 Hrs.)

SoC: Components and Architectures, Processor Cores in SoC: Soft Cores vs. Hard Cores. Communication Protocols: UART, I2c, SPI, AMBA (APB, AHB), AXI. Memory Subsystems and IP Integration. High-Level Synthesis Tools for SoC Design.

Unit IV: Emerging Trends in ASIC and SoC Design (06 Hrs.)

Low Power ASIC Design Techniques. Heterogeneous SoC Architectures, Role of Machine Learning in SoC Development, AI and ML Accelerators in SoC, Chiplets and 3D IC Integration, Hardware Acceleration using FPGA and PYNQ Boards. Green and Sustainable ASIC/SoC Design, Case Studies: Real-World Applications of ASICs and SoCs.

Textbooks & References:

1. "Application-Specific Integrated Circuits" by Michael John Sebastian Smith.
2. "CMOS VLSI Design: A Circuits and Systems Perspective" by Neil H.E. Weste and David Harris.
3. "Digital Design and Computer Architecture" by David Harris and Sarah Harris.
4. "System-on-Chip Design with Arm Cortex-M Processors" by Joseph Yiu.
5. MATLAB and Micro wind Tool Manuals.

Practical Syllabus

All practicals to be performed using Micro wind software.

1. Introduction to Micro wind: Design and simulate CMOS inverter, NAND and NOR layout.
2. Design and simulate Half Adder & Full Adder
3. Design and Simulate 2:1 Mux using logic gates & transmission gates
4. Design and Simulate One-bit SRAM Cell
5. Develop a project to implement any System on Chip using Simulink, HDL Coder and FPGA Board

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